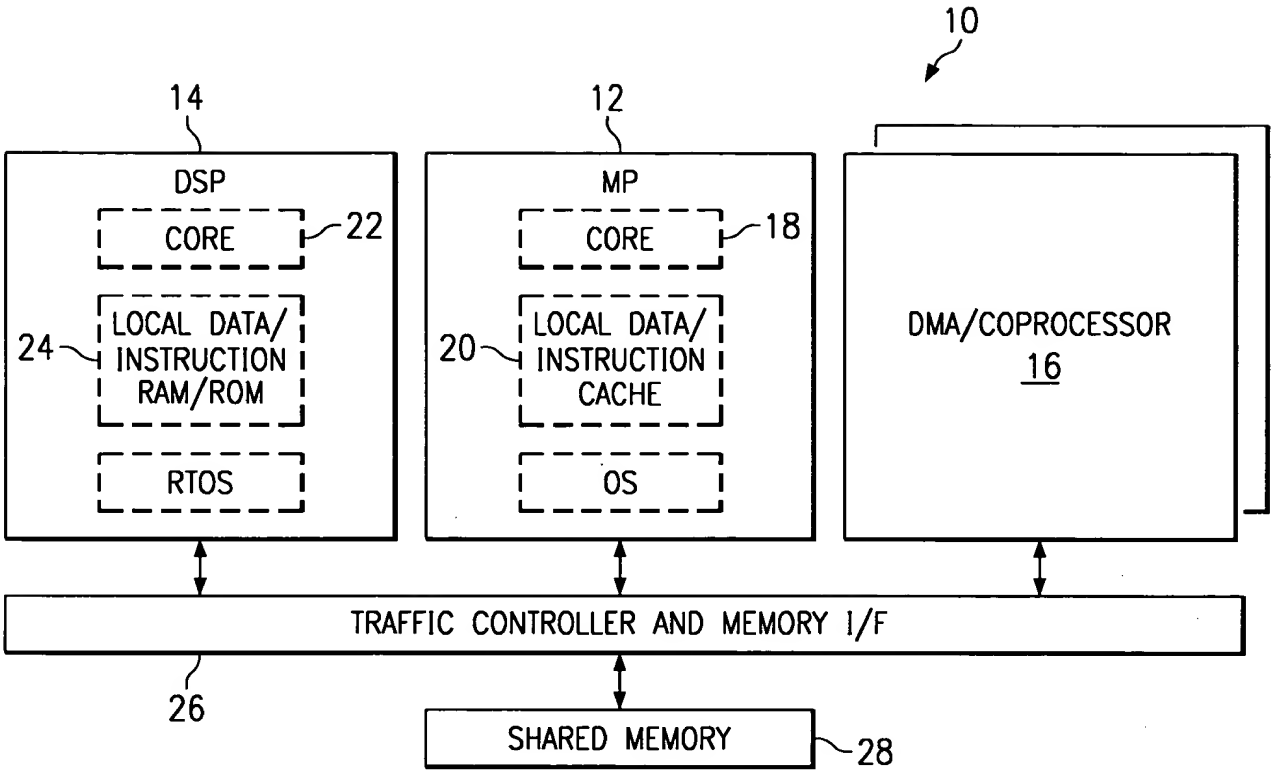
10
14
12
DSP
CORE
22
LOCAL DATA/
INSTRUCTION
RAM/ROM
24
RTOS
MP
CORE
18
LOCAL DATA/
INSTRUCTION
CACHE
20
OS
DMA/COPROCESSOR
16
TRAFFIC CONTROLLER AND MEMORY I/F
26
SHARED MEMORY
28

FIG. 1

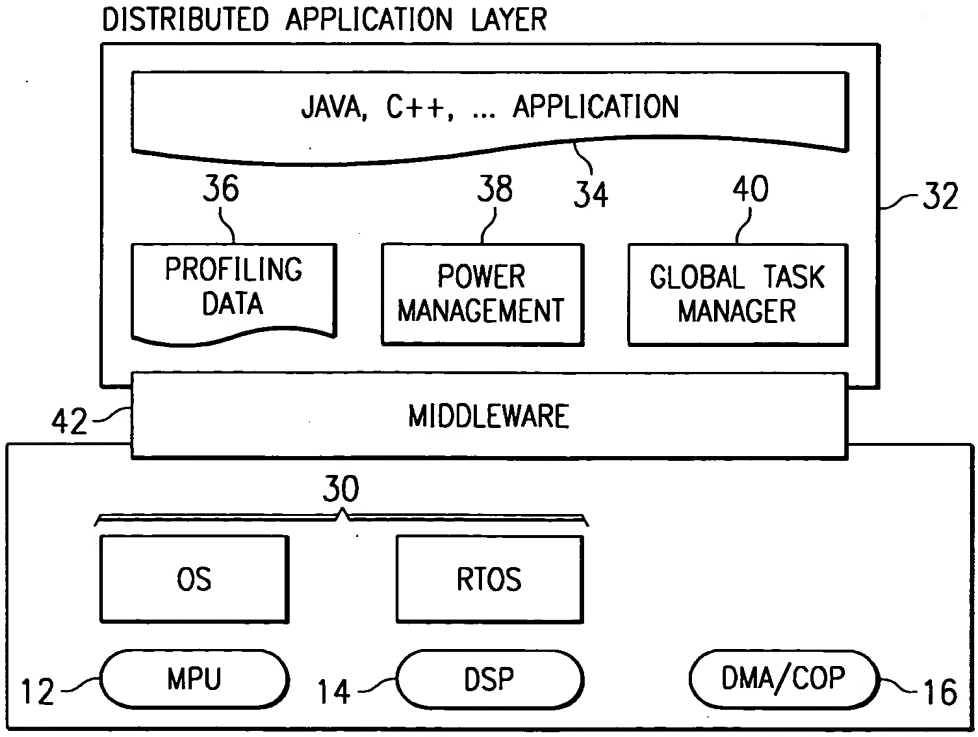
DISTRIBUTED APPLICATION LAYER
JAVA, C++, ... APPLICATION
34
36
38
40
32
PROFILING
DATA
POWER
MANAGEMENT
GLOBAL TASK
MANAGER
42
MIDDLEWARE
30
OS
RTOS
12
MPU
14
DSP
DMA/COP
16

FIG. 2

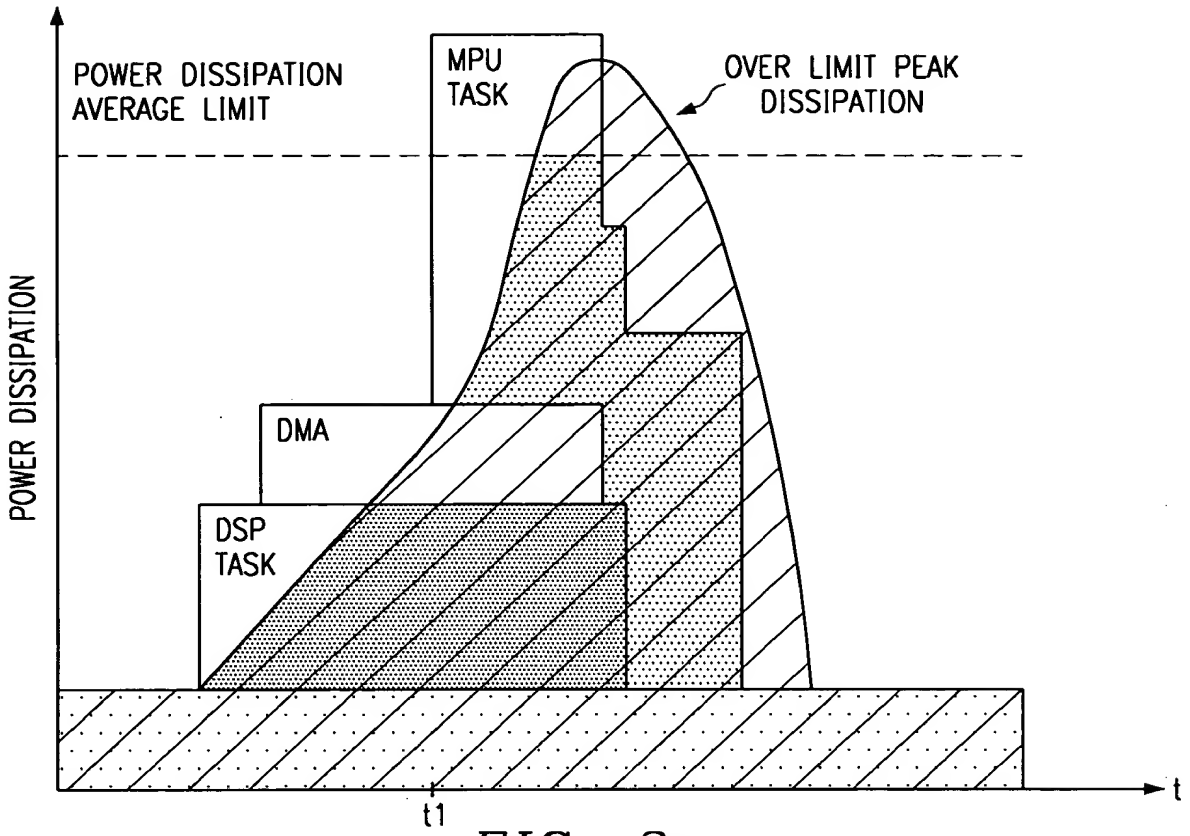
POWER DISSIPATION
AVERAGE LIMIT
MPU
TASK
OVER LIMIT PEAK
DISSIPATION
POWER DISSIPATION
DMA
DSP
TASK
t1
t

FIG. 3a

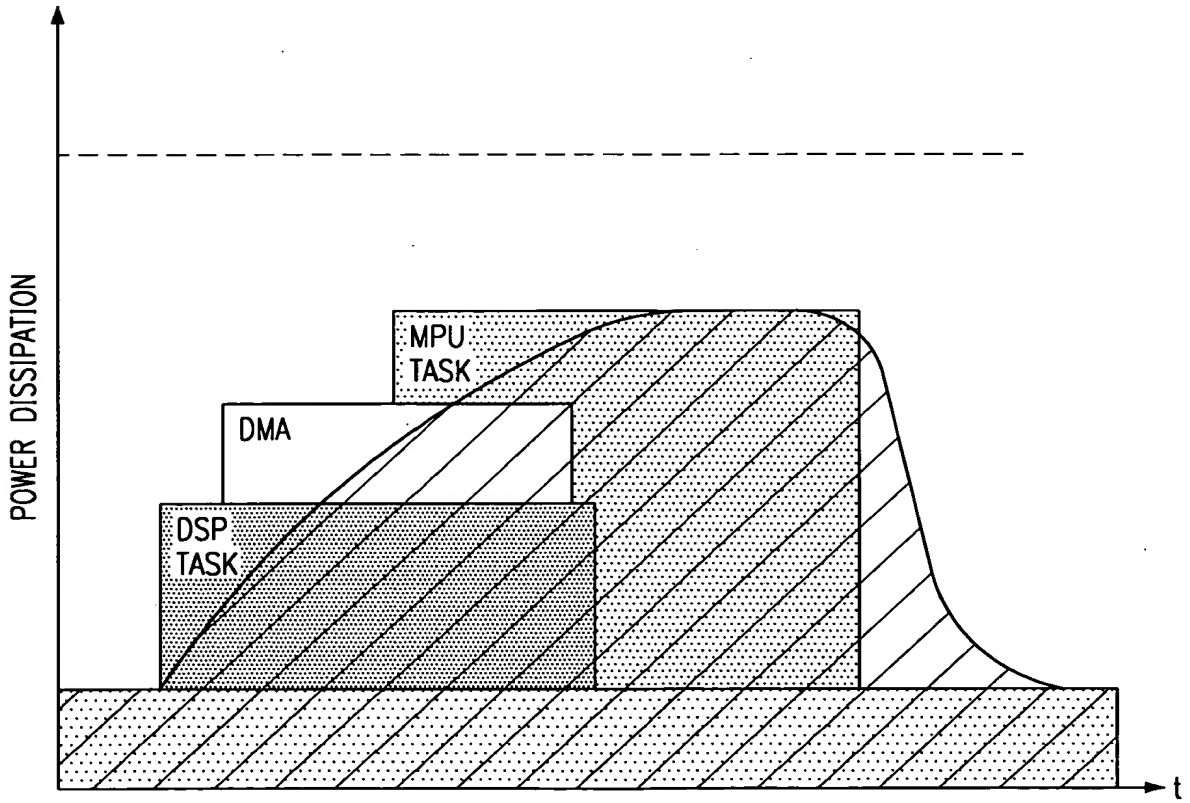
POWER DISSIPATION
MPU
TASK
DMA
DSP
TASK
t

FIG. 3b

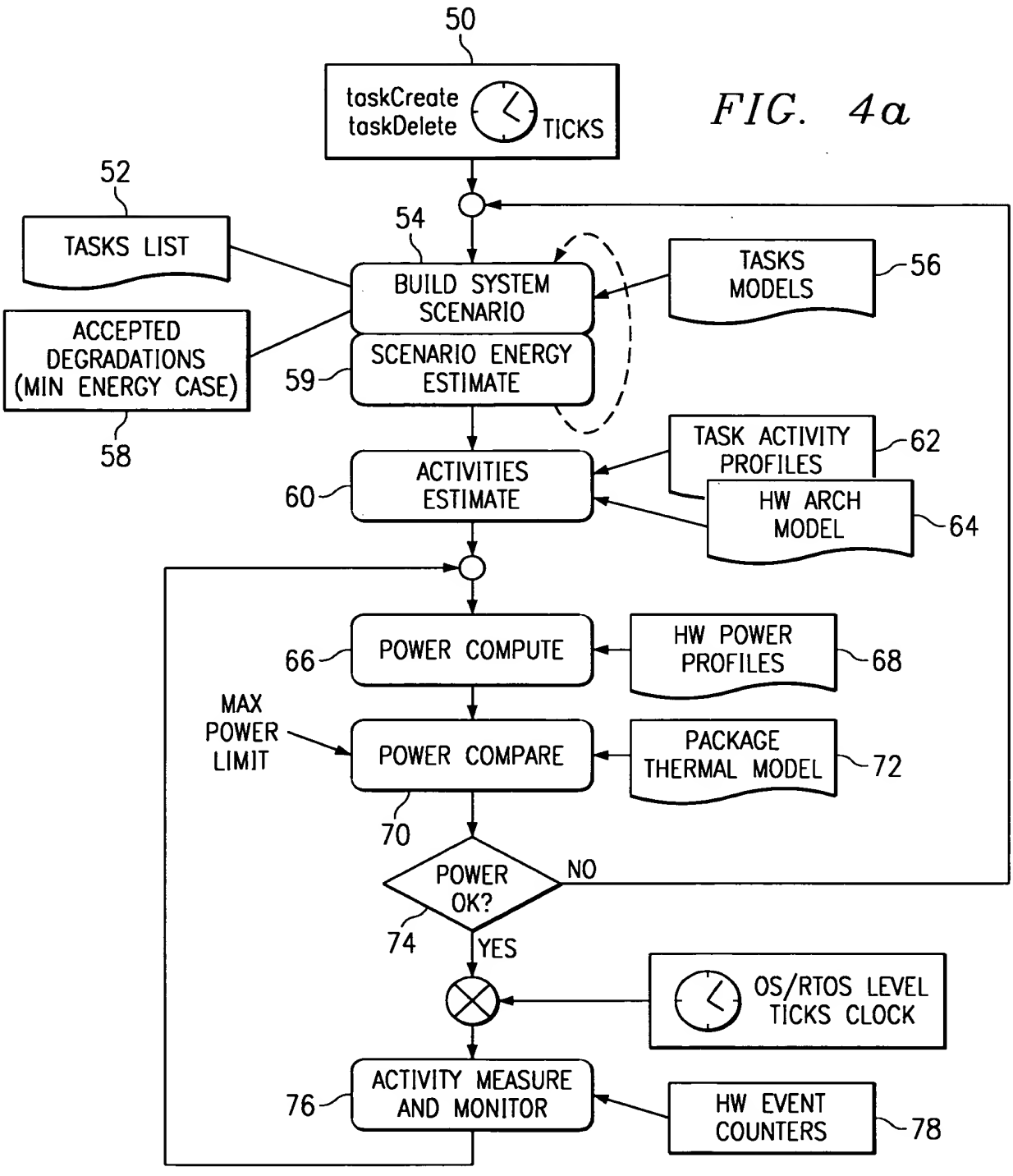
50
taskCreate
taskDelete
TICKS
52
TASKS LIST
54
BUILD SYSTEM SCENARIO
TASKS MODELS
56
ACCEPTED DEGRADATIONS (MIN ENERGY CASE)
58
59
SCENARIO ENERGY ESTIMATE
TASK ACTIVITY PROFILES
62
60
ACTIVITIES ESTIMATE
HW ARCH MODEL
64
66
POWER COMPUTE
HW POWER PROFILES
68
MAX POWER LIMIT
POWER COMPARE
PACKAGE THERMAL MODEL
72
70
POWER OK?
NO
74
YES
OS/RTOS LEVEL TICKS CLOCK
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78

FIG. 4a

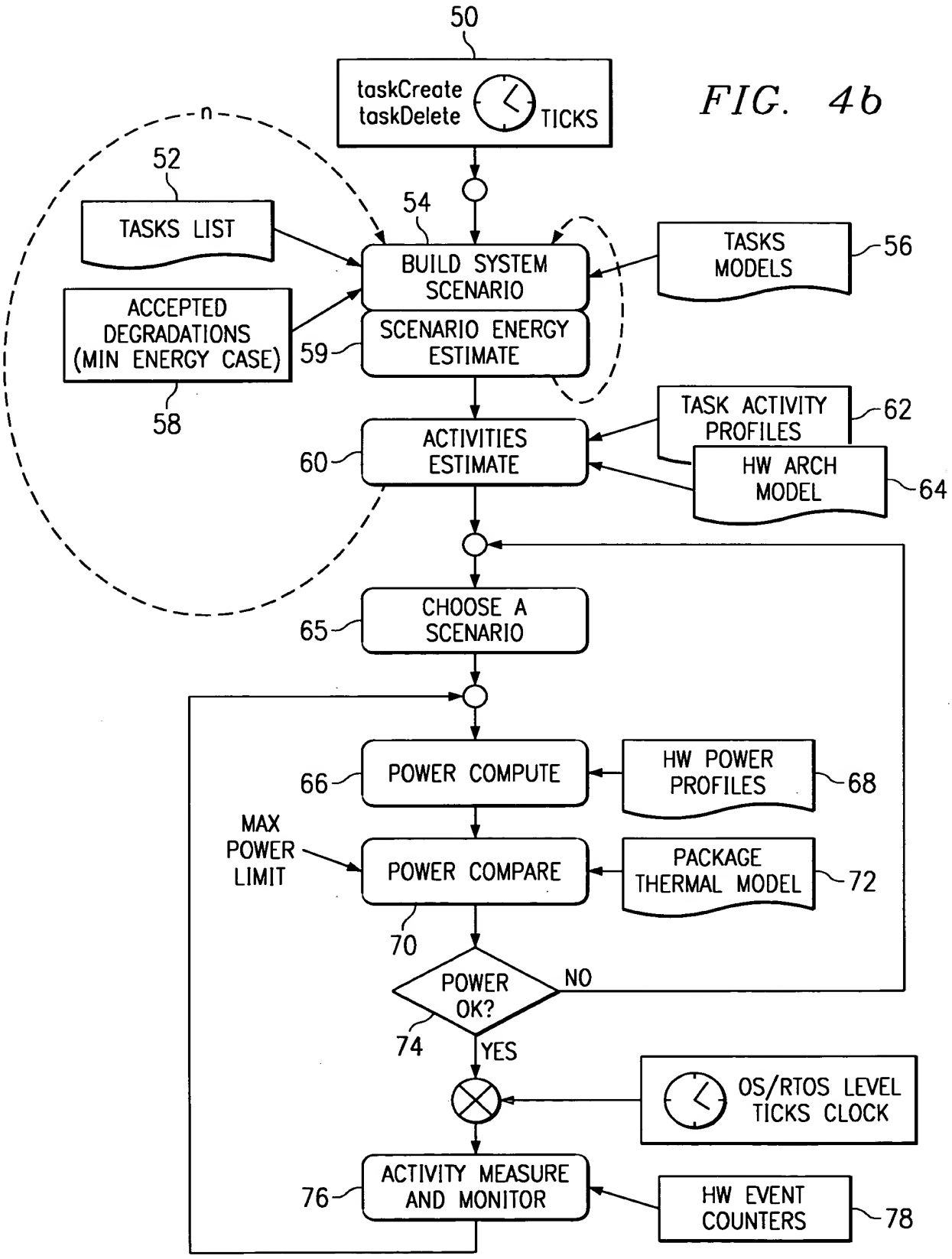
50
taskCreate
taskDelete
TICKS
n
52
TASKS LIST
54
BUILD SYSTEM SCENARIO
TASKS MODELS
56
ACCEPTED DEGRADATIONS (MIN ENERGY CASE)
58
59
SCENARIO ENERGY ESTIMATE
TASK ACTIVITY PROFILES
62
60
ACTIVITIES ESTIMATE
HW ARCH MODEL
64
65
CHOOSE A SCENARIO
66
POWER COMPUTE
HW POWER PROFILES
68
MAX POWER LIMIT
POWER COMPARE
PACKAGE THERMAL MODEL
72
70
POWER OK?
NO
74
YES
OS/RTOS LEVEL TICKS CLOCK
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78

FIG. 4b

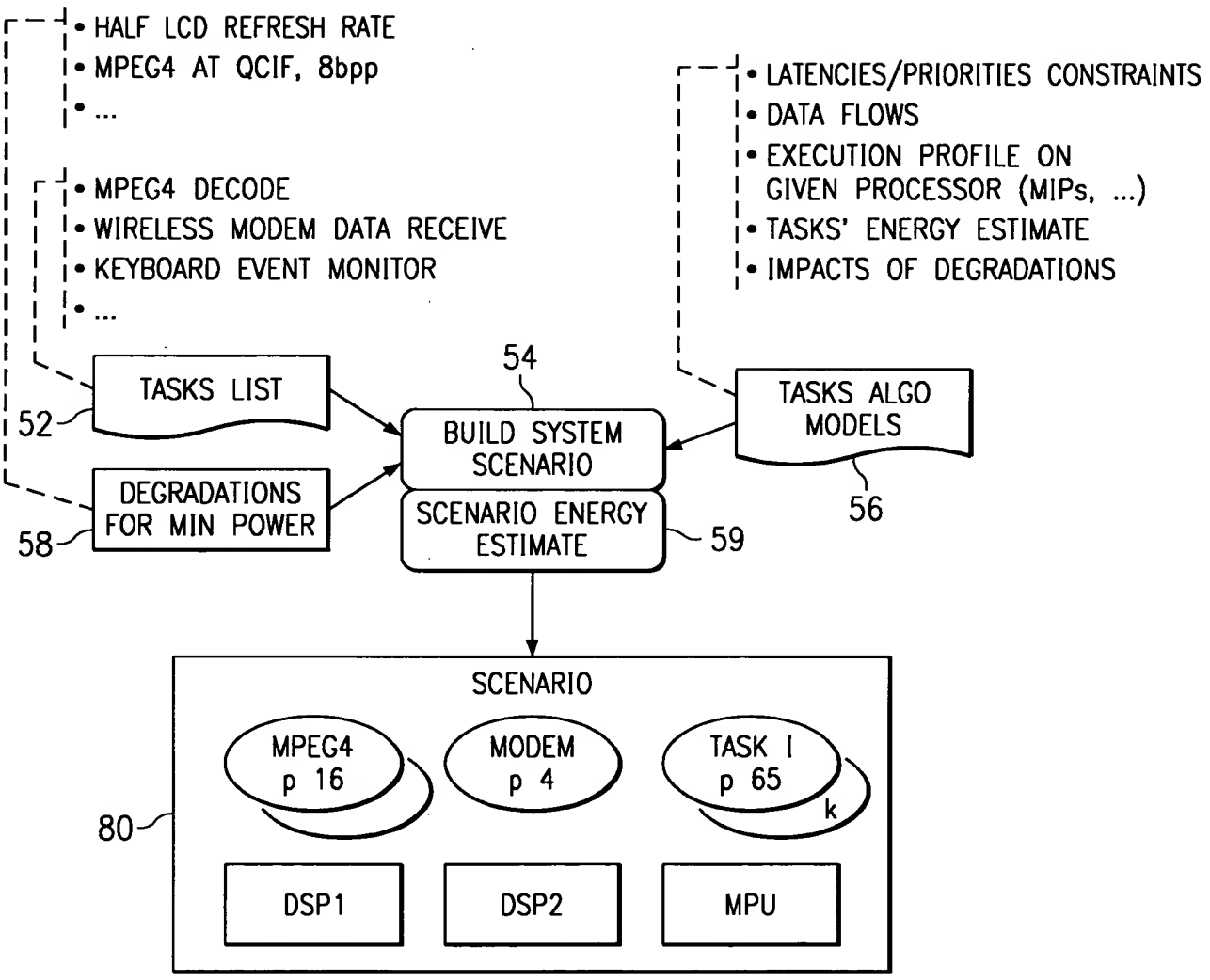
• HALF LCD REFRESH RATE
• MPEG4 AT QCIF, 8bpp
• ...
• MPEG4 DECODE
• WIRELESS MODEM DATA RECEIVE
• KEYBOARD EVENT MONITOR
• ...
• LATENCIES/PRIORITIES CONSTRAINTS
• DATA FLOWS
• EXECUTION PROFILE ON GIVEN PROCESSOR (MIPs, ...)
• TASKS' ENERGY ESTIMATE
• IMPACTS OF DEGRADATIONS
TASKS LIST
52
DEGRADATIONS FOR MIN POWER
58
54
BUILD SYSTEM SCENARIO
SCENARIO ENERGY ESTIMATE
59
TASKS ALGO MODELS
56
SCENARIO
MPEG4 p 16
MODEM p 4
TASK I p 65
k
80
DSP1
DSP2
MPU

FIG. 5

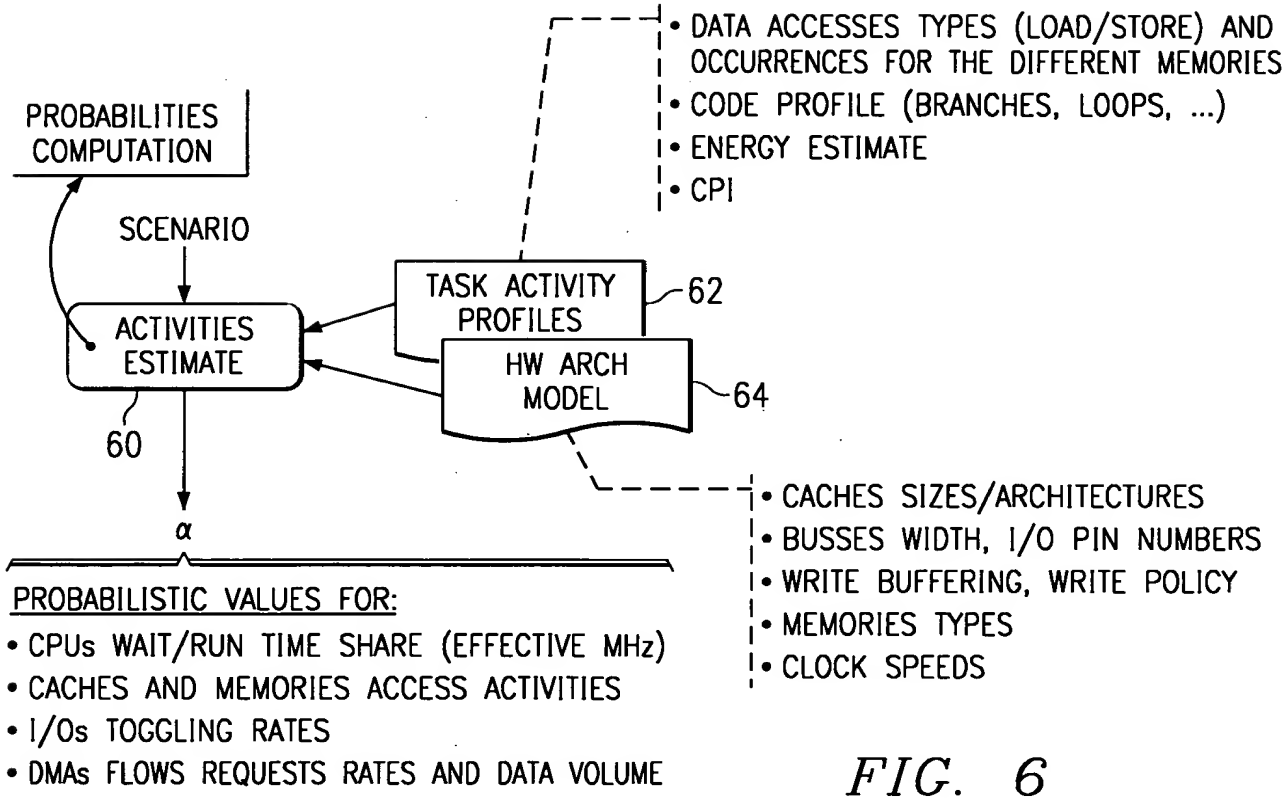
PROBABILITIES COMPUTATION
SCENARIO
ACTIVITIES ESTIMATE
60
α
TASK ACTIVITY PROFILES
62
HW ARCH MODEL
64
• DATA ACCESSES TYPES (LOAD/STORE) AND OCCURRENCES FOR THE DIFFERENT MEMORIES
• CODE PROFILE (BRANCHES, LOOPS, ...)
• ENERGY ESTIMATE
• CPI
• CACHES SIZES/ARCHITECTURES
• BUSSES WIDTH, I/O PIN NUMBERS
• WRITE BUFFERING, WRITE POLICY
• MEMORIES TYPES
• CLOCK SPEEDS
PROBABILISTIC VALUES FOR:
• CPUs WAIT/RUN TIME SHARE (EFFECTIVE MHz)
• CACHES AND MEMORIES ACCESS ACTIVITIES
• I/Os TOGGLING RATES
• DMAs FLOWS REQUESTS RATES AND DATA VOLUME

FIG. 6

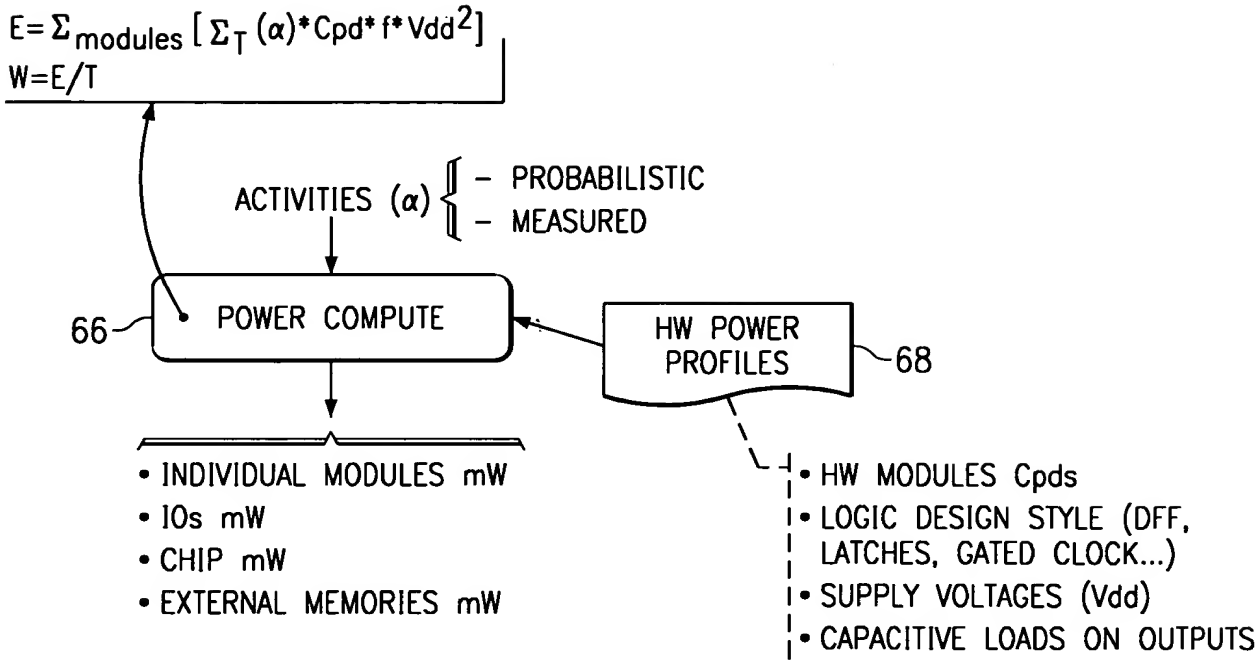
E=Σmodules [ΣT (α)*Cpd* f* Vdd2]
W=E/T
ACTIVITIES (α)
– PROBABILISTIC
– MEASURED
66
POWER COMPUTE
HW POWER PROFILES
68
• INDIVIDUAL MODULES mW
• IOs mW
• CHIP mW
• EXTERNAL MEMORIES mW
• HW MODULES Cpds
• LOGIC DESIGN STYLE (DFF, LATCHES, GATED CLOCK...)
• SUPPLY VOLTAGES (Vdd)
• CAPACITIVE LOADS ON OUTPUTS

FIG. 7

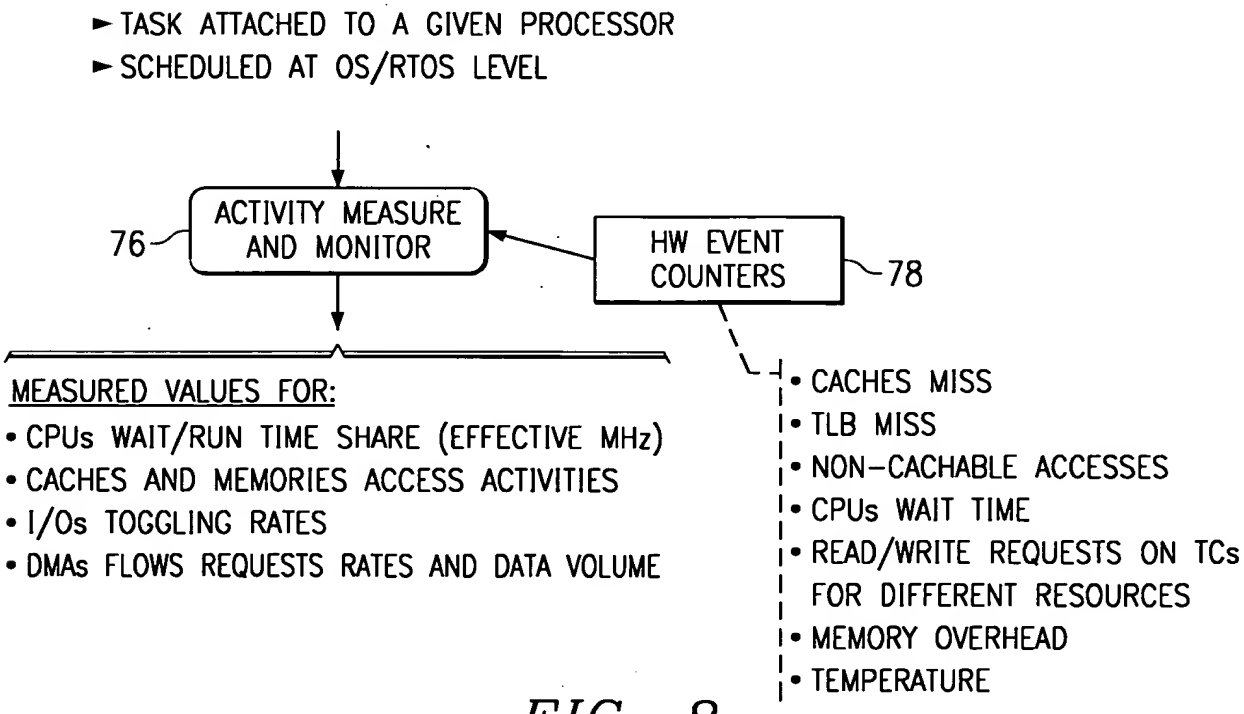
► TASK ATTACHED TO A GIVEN PROCESSOR
► SCHEDULED AT OS/RTOS LEVEL
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78
MEASURED VALUES FOR:
• CPUs WAIT/RUN TIME SHARE (EFFECTIVE MHz)
• CACHES AND MEMORIES ACCESS ACTIVITIES
• I/Os TOGGLING RATES
• DMAs FLOWS REQUESTS RATES AND DATA VOLUME
• CACHES MISS
• TLB MISS
• NON–CACHABLE ACCESSES
• CPUs WAIT TIME
• READ/WRITE REQUESTS ON TCs FOR DIFFERENT RESOURCES
• MEMORY OVERHEAD
• TEMPERATURE

FIG. 8

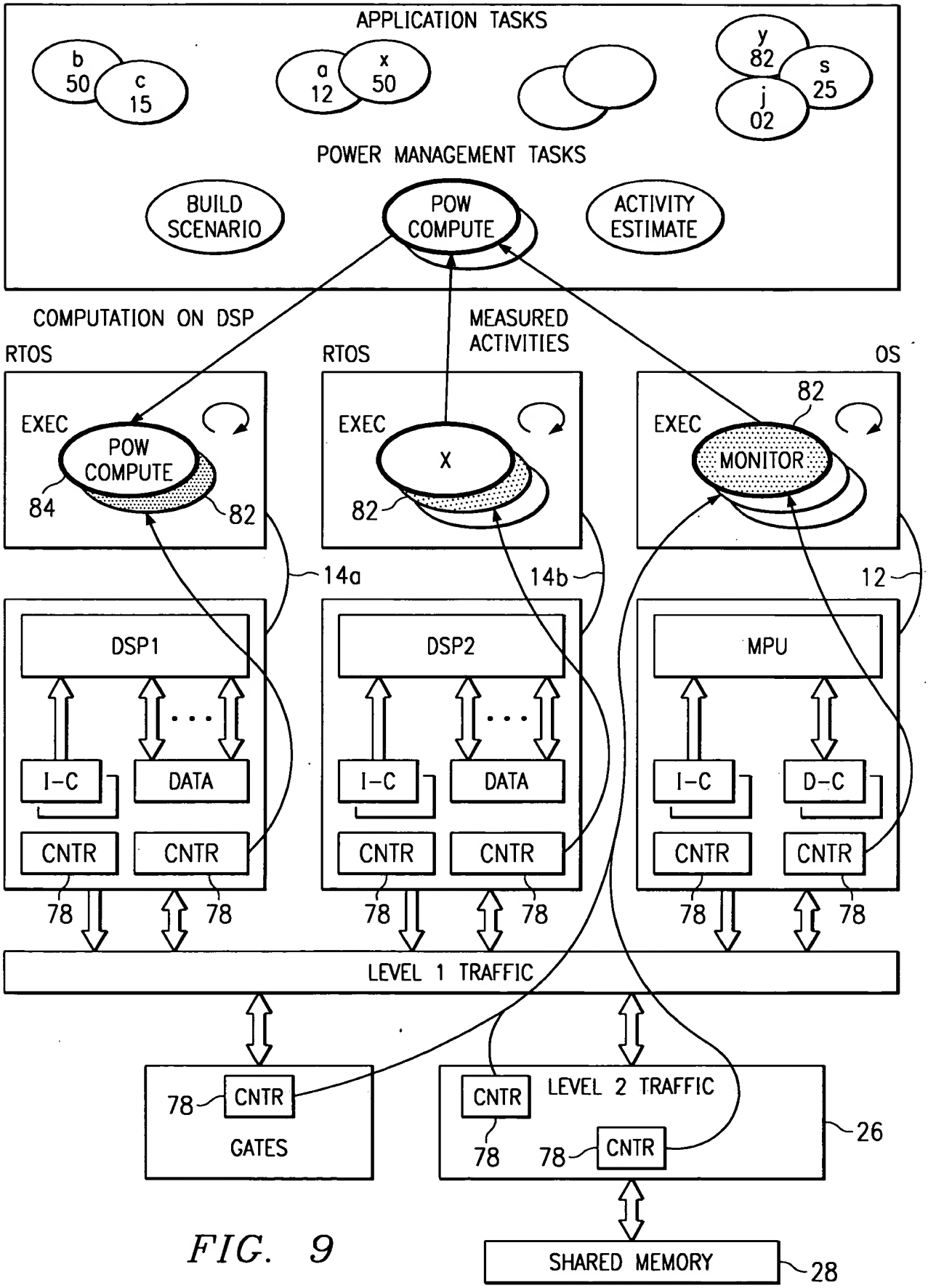
APPLICATION TASKS
b
50
c
15
a
12
x
50
y
82
s
25
j
02
POWER MANAGEMENT TASKS
BUILD SCENARIO
POW COMPUTE
ACTIVITY ESTIMATE
COMPUTATION ON DSP
MEASURED ACTIVITIES
RTOS
RTOS
OS
EXEC
POW COMPUTE
84
82
EXEC
X
82
EXEC
82
MONITOR
14a
14b
12
DSP1
DSP2
MPU
I-C
DATA
I-C
DATA
I-C
D-C
CNTR
CNTR
CNTR
CNTR
CNTR
CNTR
78
78
78
78
78
78
LEVEL 1 TRAFFIC
78
CNTR
GATES
CNTR
LEVEL 2 TRAFFIC
78
78
CNTR
26
SHARED MEMORY
28

FIG. 9

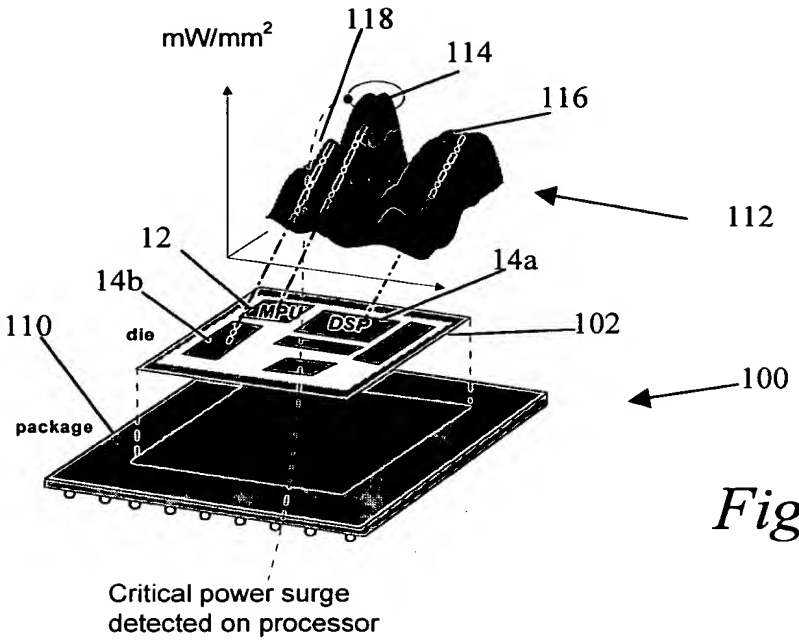
mW/mm²
118
114
116
112
12
14b
14a
110
die
MPU
DSP
102
100
package
Critical power surge
detected on processor

Fig. 10

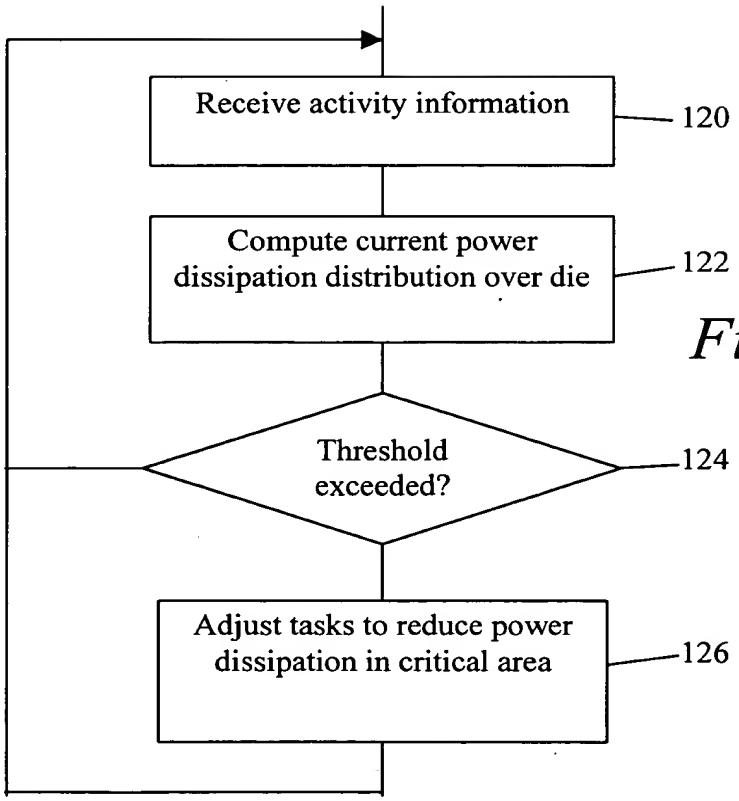
Receive activity information
120
Compute current power dissipation distribution over die
122
Threshold exceeded?
124
Adjust tasks to reduce power dissipation in critical area
126

Fig. 11

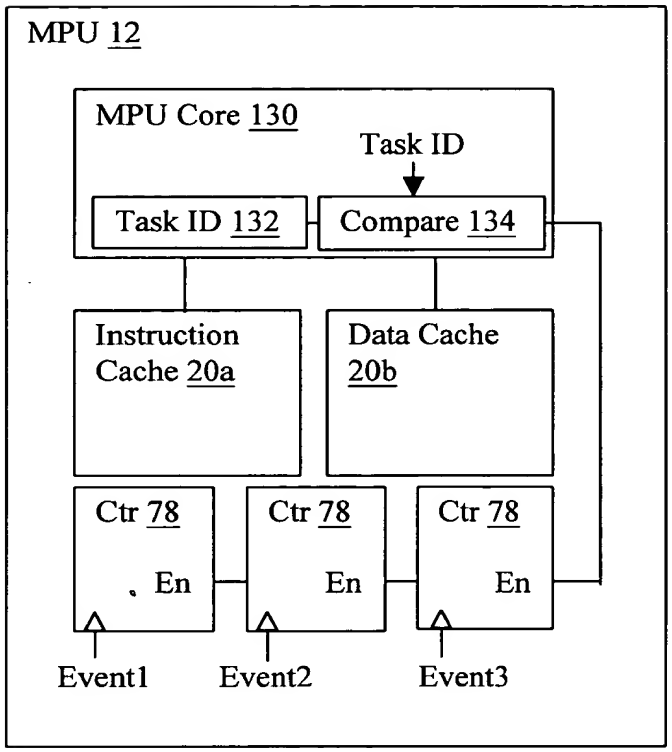
MPU 12
MPU Core 130
Task ID
Task ID 132
Compare 134
Instruction Cache 20a
Data Cache 20b
Ctr 78
En
Ctr 78
En
Ctr 78
En
Event1
Event2
Event3

Fig. 12

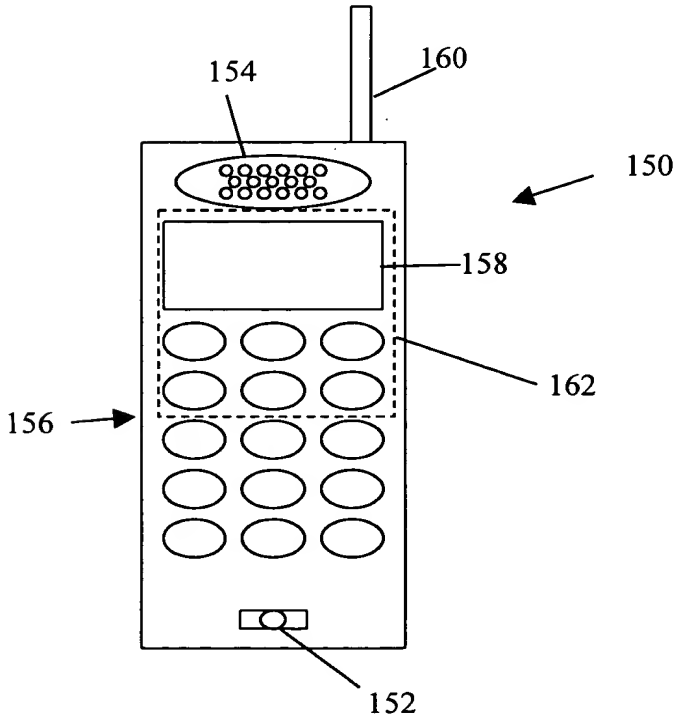
154
160
150
158
162
156
152

Fig. 13